

3次元積層製造技術開発のためのウエハ

Wafer for 3D-stack Research and Development

TSV + Bump wafer

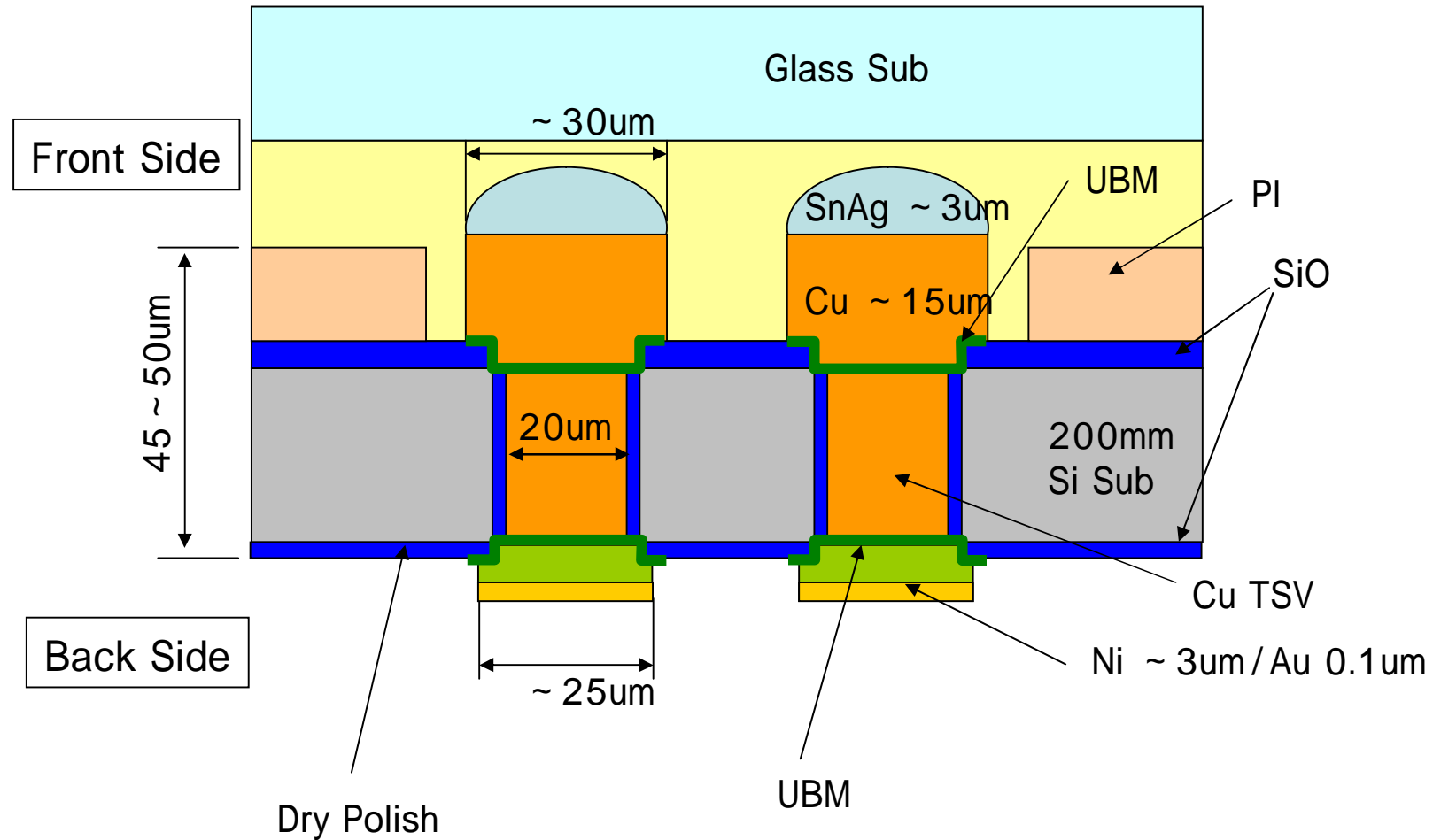
Wafer bonding

TSV wafer / glass bonding

PET film / glass bonding

TSV Bump TEG (Custom Pattern)

Via First TSV Wafer with Double Side Bump



TSV Si Etch test wafer

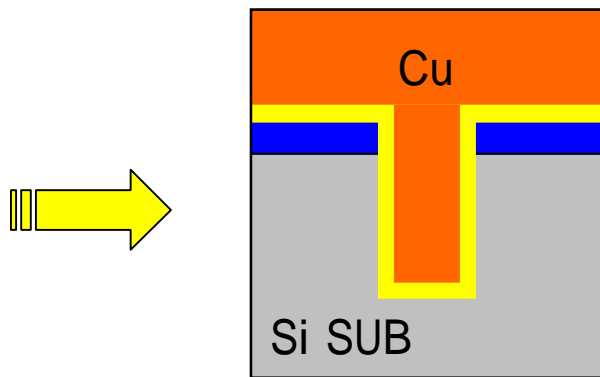
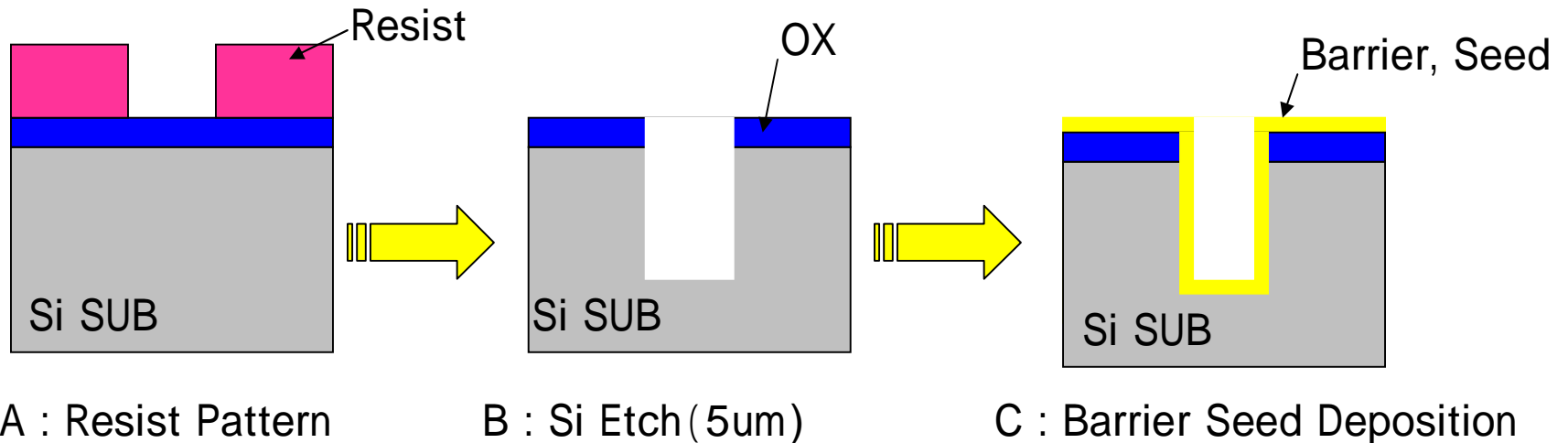
process	Wafer Size	Mask	Pattern Size	Chip Open Area	Remarks
Resist Mask (3.5um ~ 4um)	200mm	PT002	2um ~ 1000um	20%	Square Hole & Trench
		PT012	8um ~ 100um	8.7%	Circle Hole & Trench
	300mm	PT002 - 02	2um ~ 1000um	20%	Square Hole & Trench
Ox Hard Mask (0.5um ~ 1.5um)	200mm	PT002	2um ~ 1000um	20%	Square Hole & Trench
		PT007	2um ~ 40um	5%	Octangular Hole & Trench
		PT004	0.18um ~ 900um	56%	Memory Cell, Square, Checker, Mesh, Trench
	300mm	PT002 - 02	2um ~ 1000um	20%	Square Hole & Trench
		PT004 - 02	0.18um ~ 900um	56%	Memory Cell, Square, checker, Mesh, Trench
		PT012 - 02	2um ~ 100um	8.7%	Circle Hole & Trench

TSV Test Wafer

Mask (PT002)

For more details, please contact
us through [inquiry site](#)

Mask : PT002 (Via First Process)



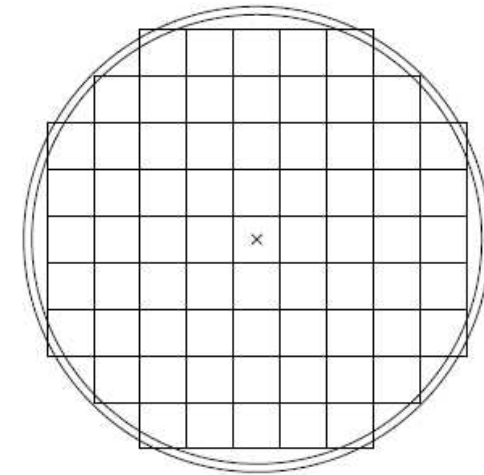
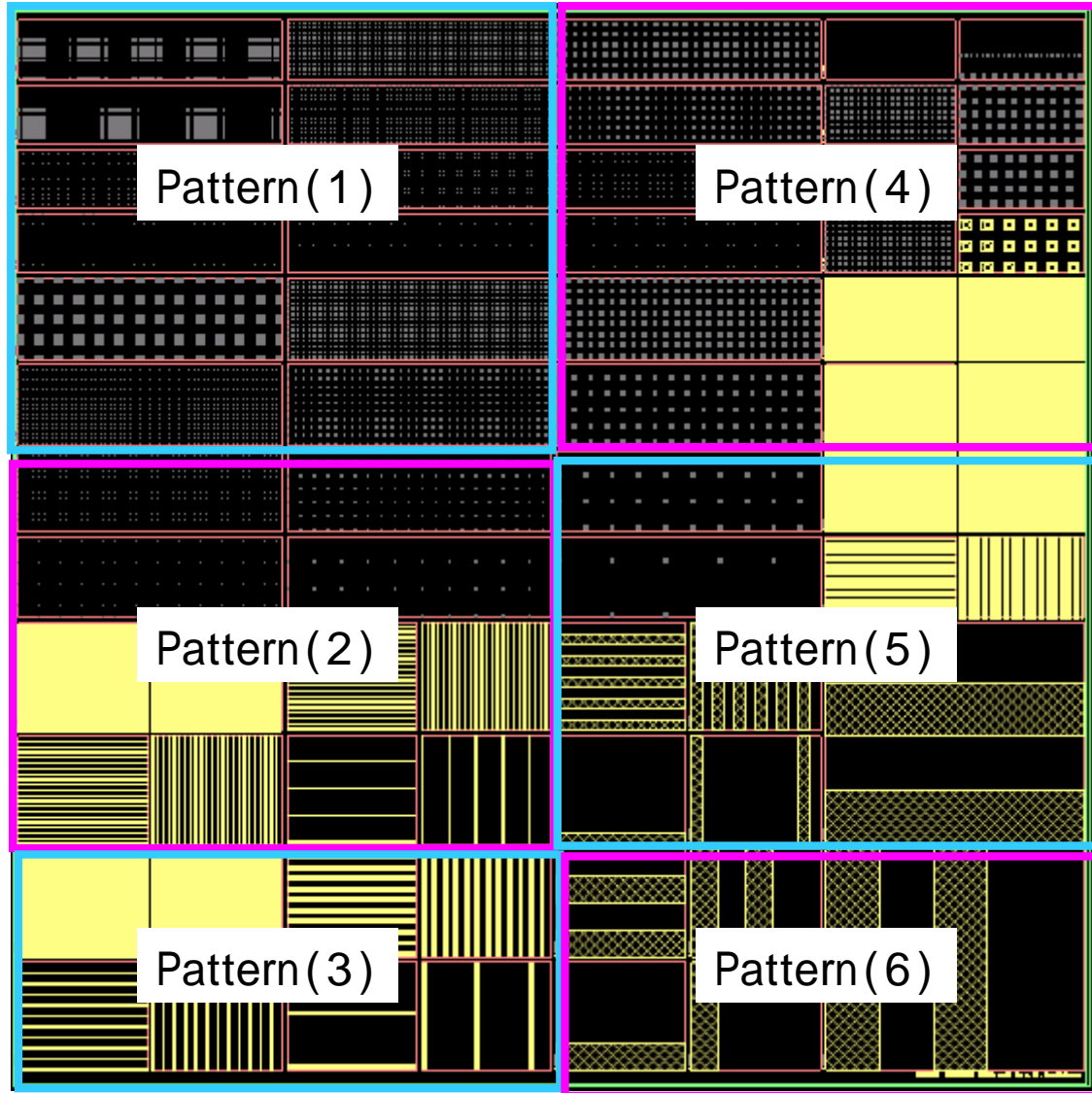
Pattern

Hole : 2um ~ 100um

Trench : 2um ~ 1000um

For Si ETCH, Cu CMP

PT002 Chip Layout



200mm Shot Map

EE 3.5mm

Chip Size 19.9mm X 19.9mm

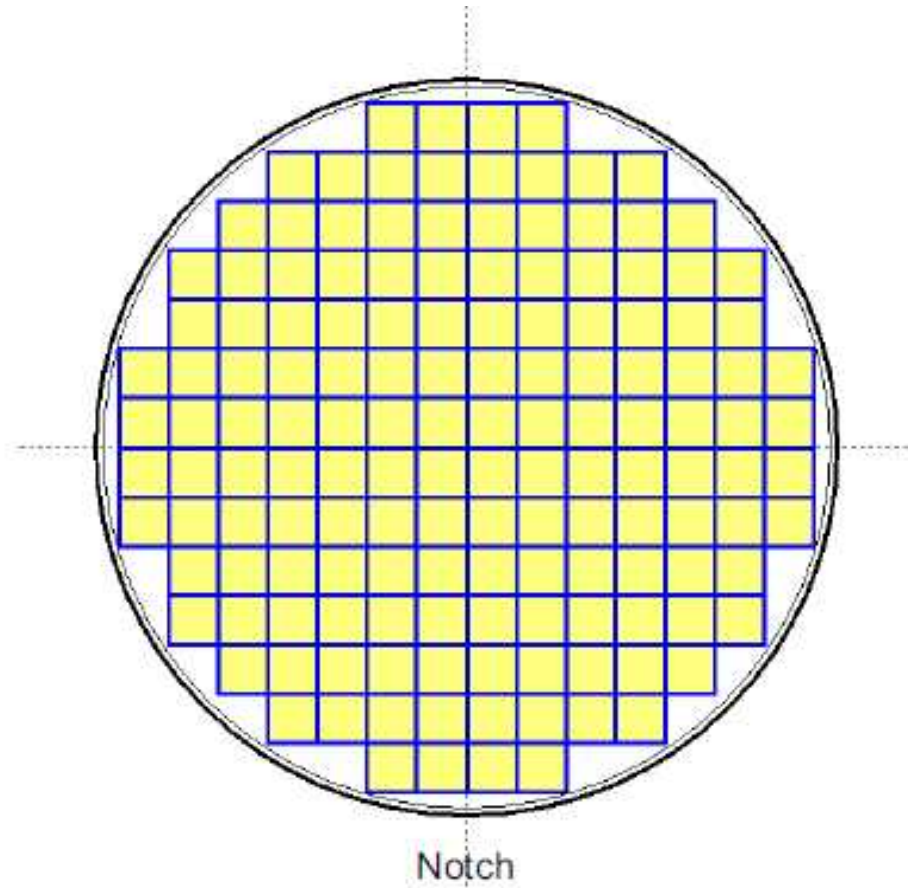
Pattern

- Hole : 2um ~ 100um
- Trench : 2um ~ 1000um

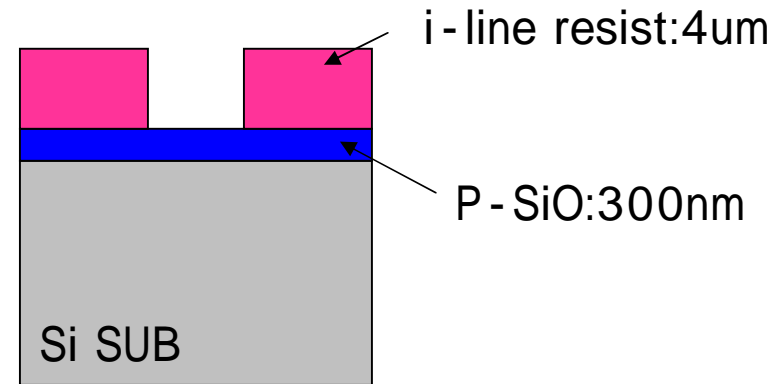
Si depth : 5um

Cu thickness : 10um, 20um

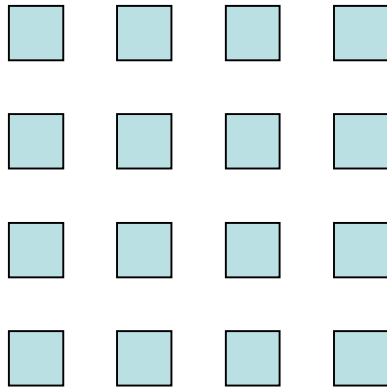
PT002 : 300mm Shot Map



Shot Map



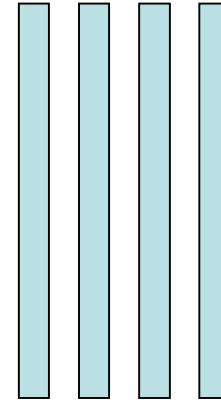
Total Shot Number : 148
Shot Array : 14 × 14
Shot Size : 20mm × 20mm
Chip Size : 19.9mm × 19.9mm



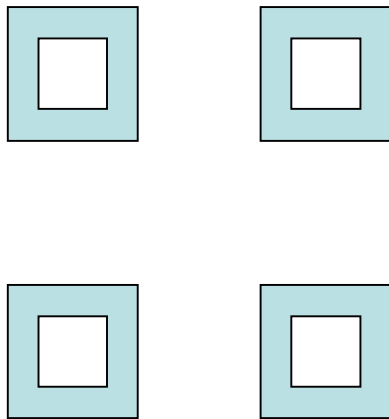
Hole Pattern



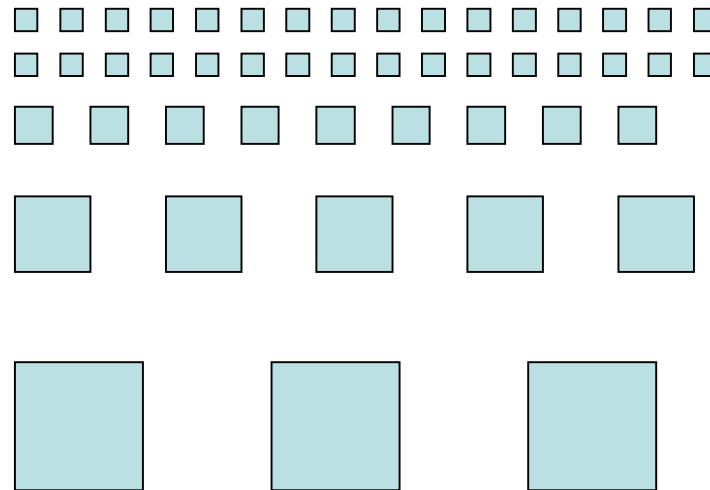
Line X Pattern



Line Y Pattern



BOX Pattern



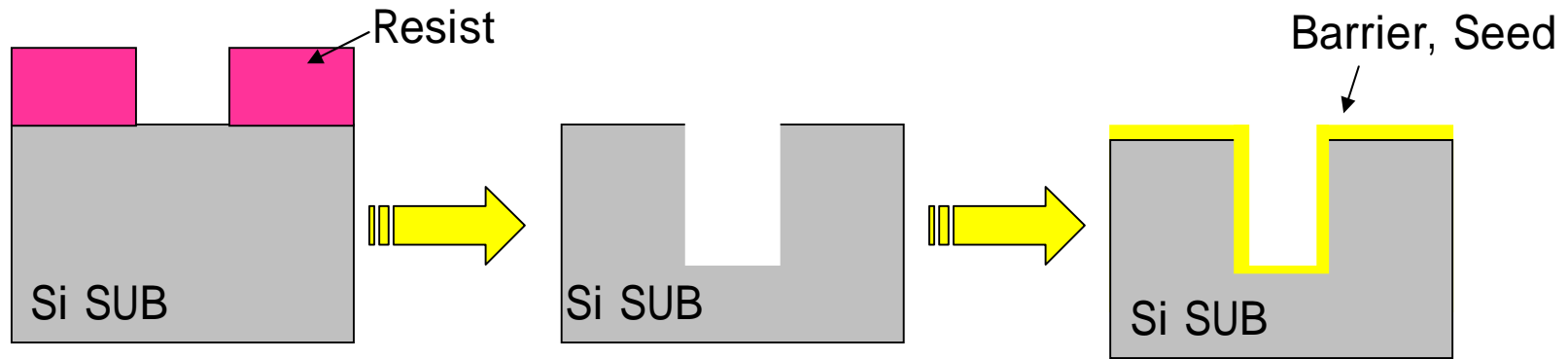
SEM Hole Pattern

TSV Test Wafer

Mask (PT012)

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us through [inquiry site](#)

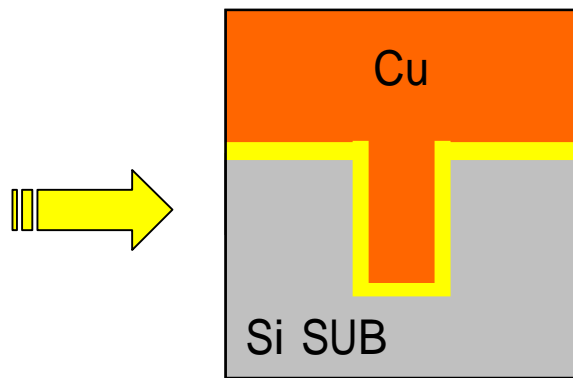
Mask : PT012 (Via First Process)



A : Resist Pattern

B : Si Bosch Etch(~ 5um)

C : Barrier Seed Deposition



D : Cu ECP

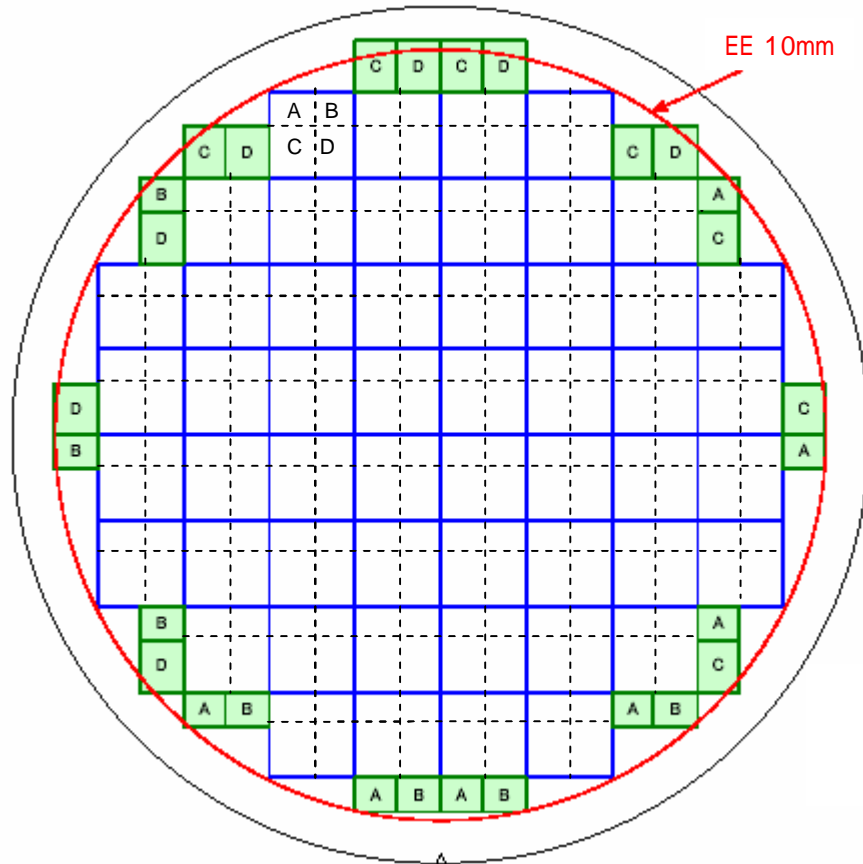
Pattern

Hole : 8um ~ 100um

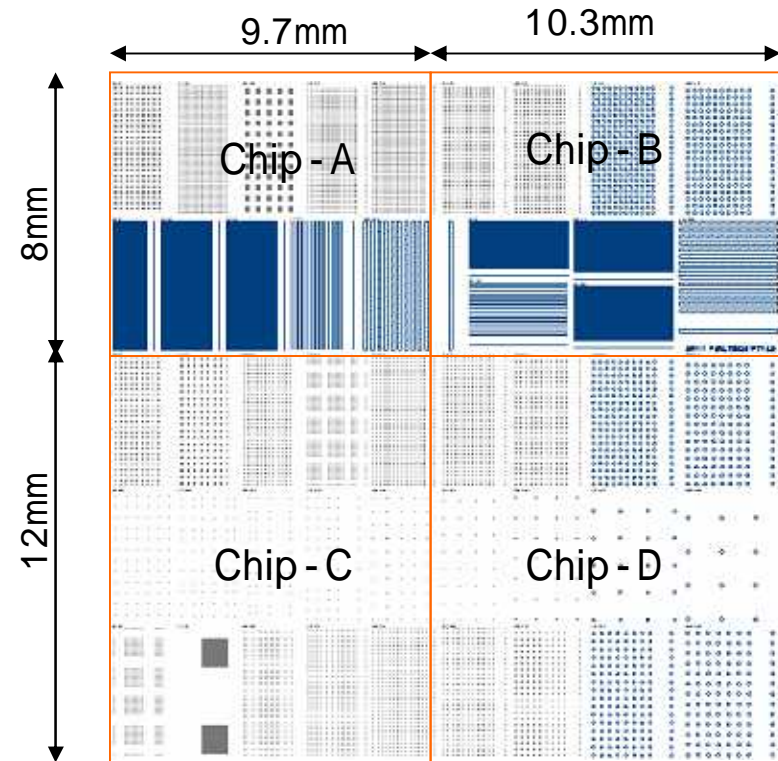
Trench : 8um ~ 100um

For Si ETCH, Cu CMP

PT012 : 200mm Shot Map

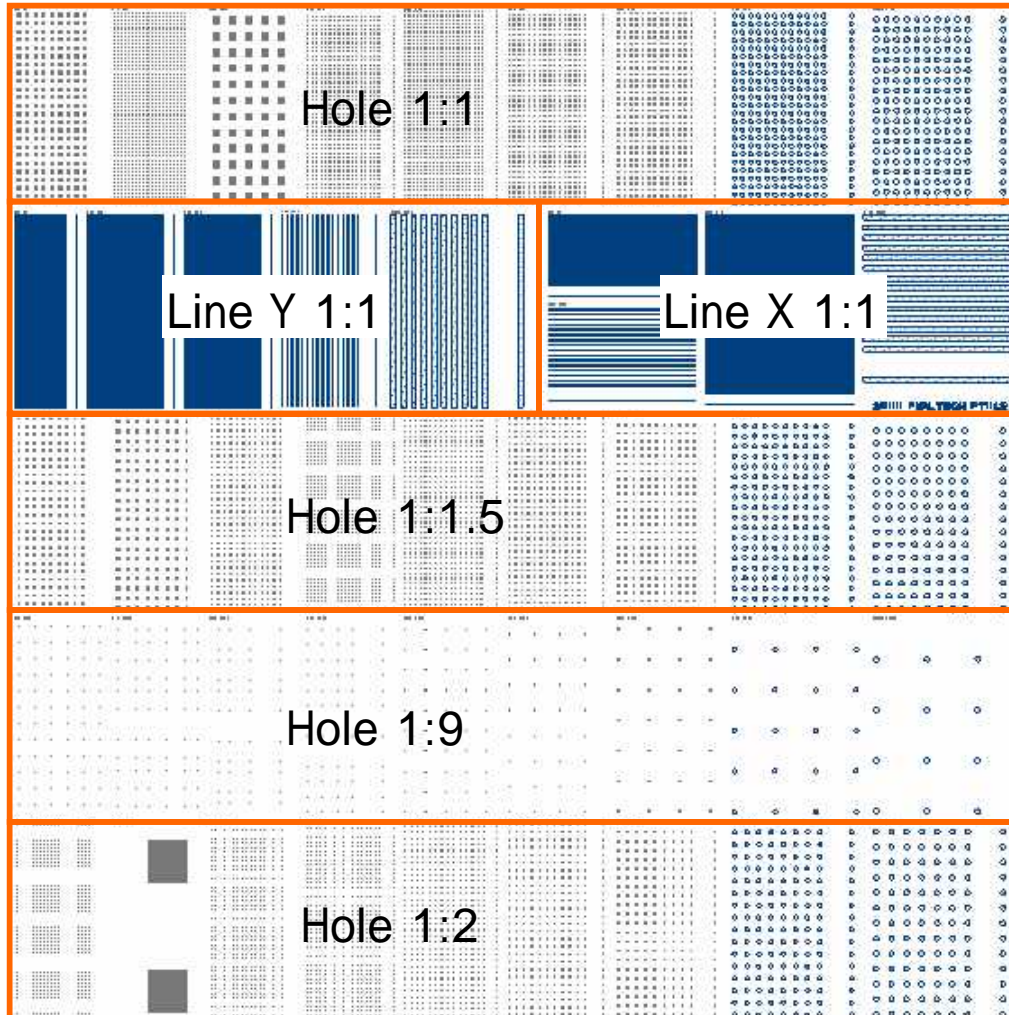


Shot Map

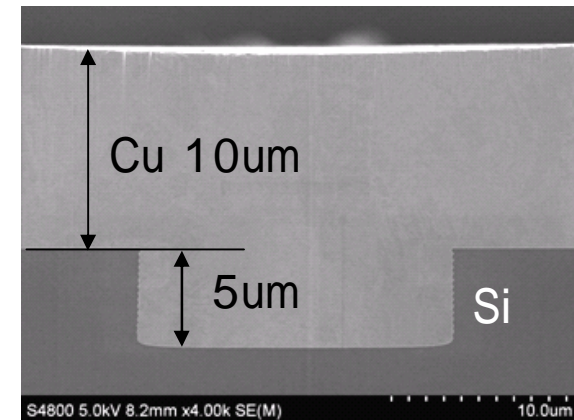


Chip Image

PT012 for TSV test (Cu CMP)

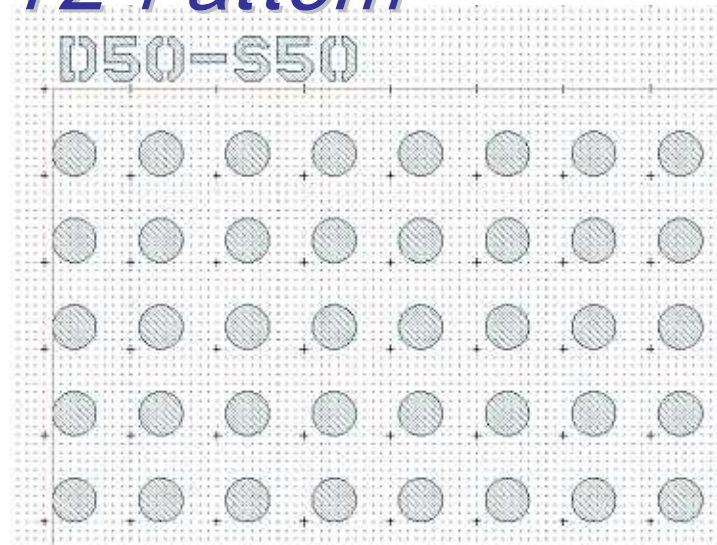


- Chip Size 20mm X 20mm
- Pattern
 - Hole : 8um ~ 100um
 - Trench : 8um ~ 100um
- Si depth : 5um
- Cu thickness : 10um

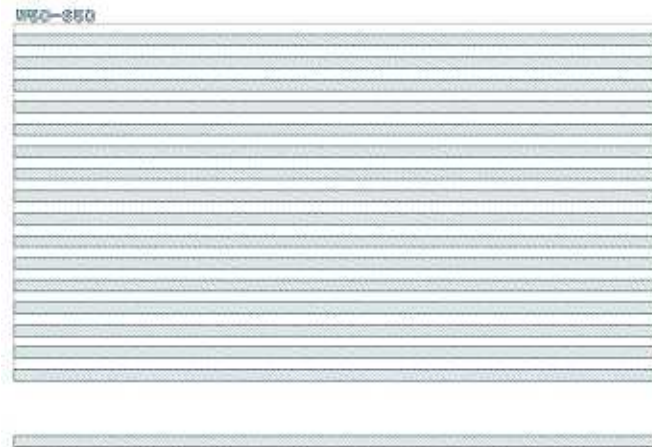


Cross Section

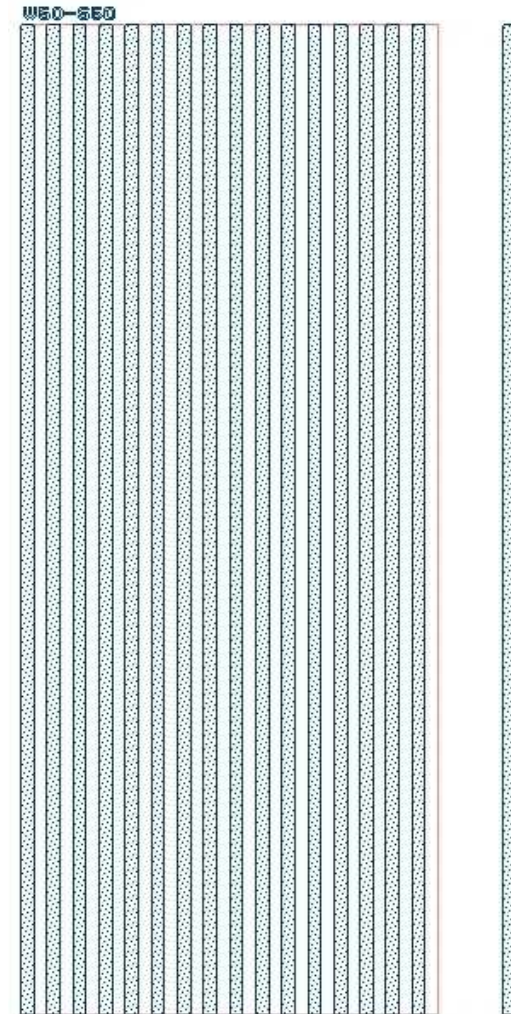
PT012 Pattern



Hole Pattern

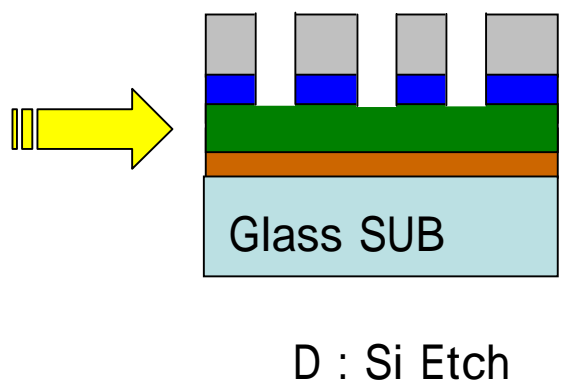
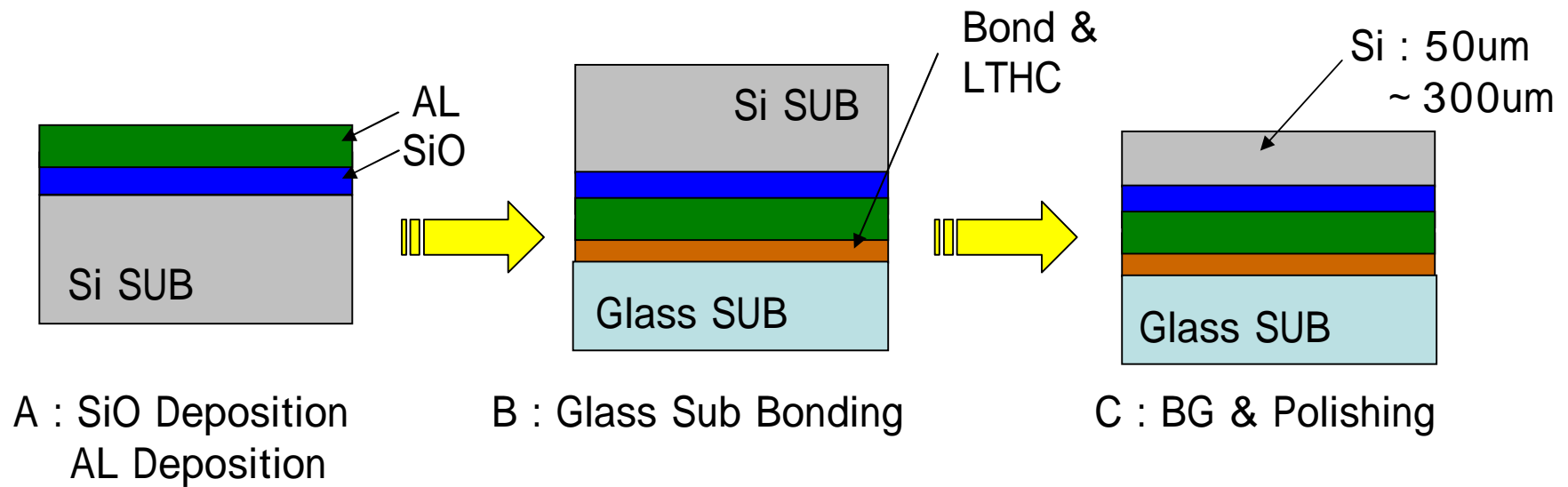


Line X Pattern



Line Y Pattern

Mask : PT012 (Via Last Process)



Pattern
Hole : 8um ~ 100um
Trench : 8um ~ 100um

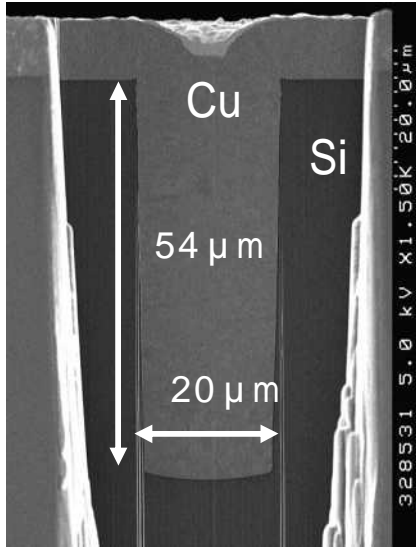
For Cu ECP

TSV Test Wafer

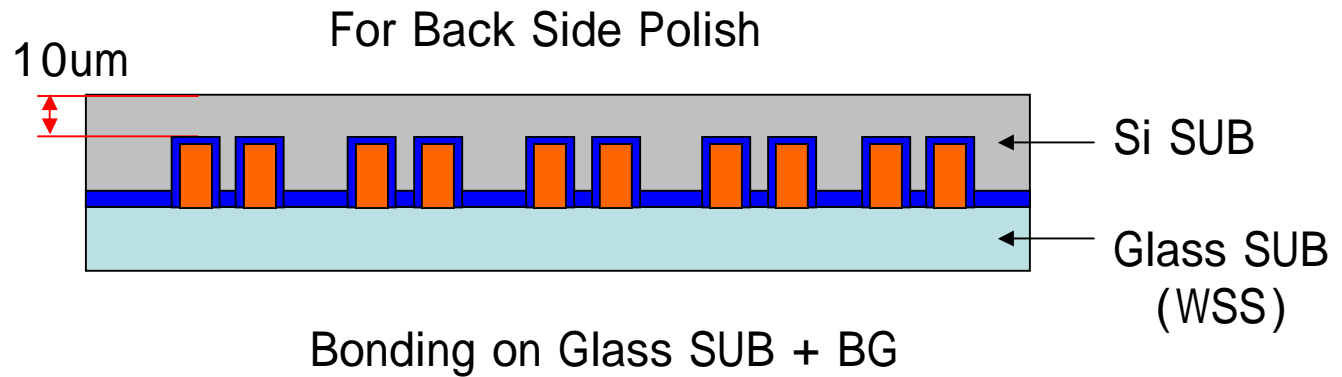
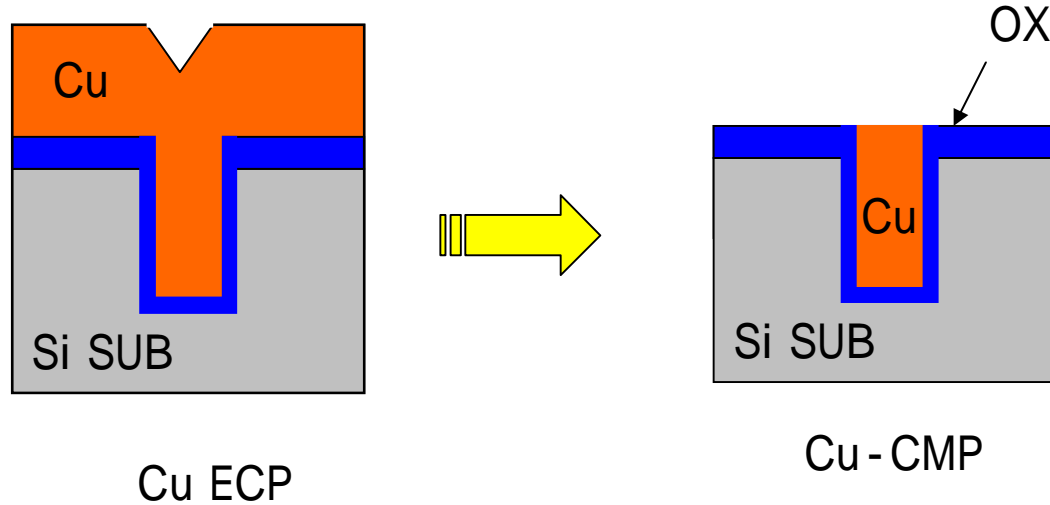
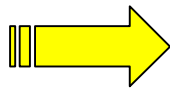
Mask (PT007)

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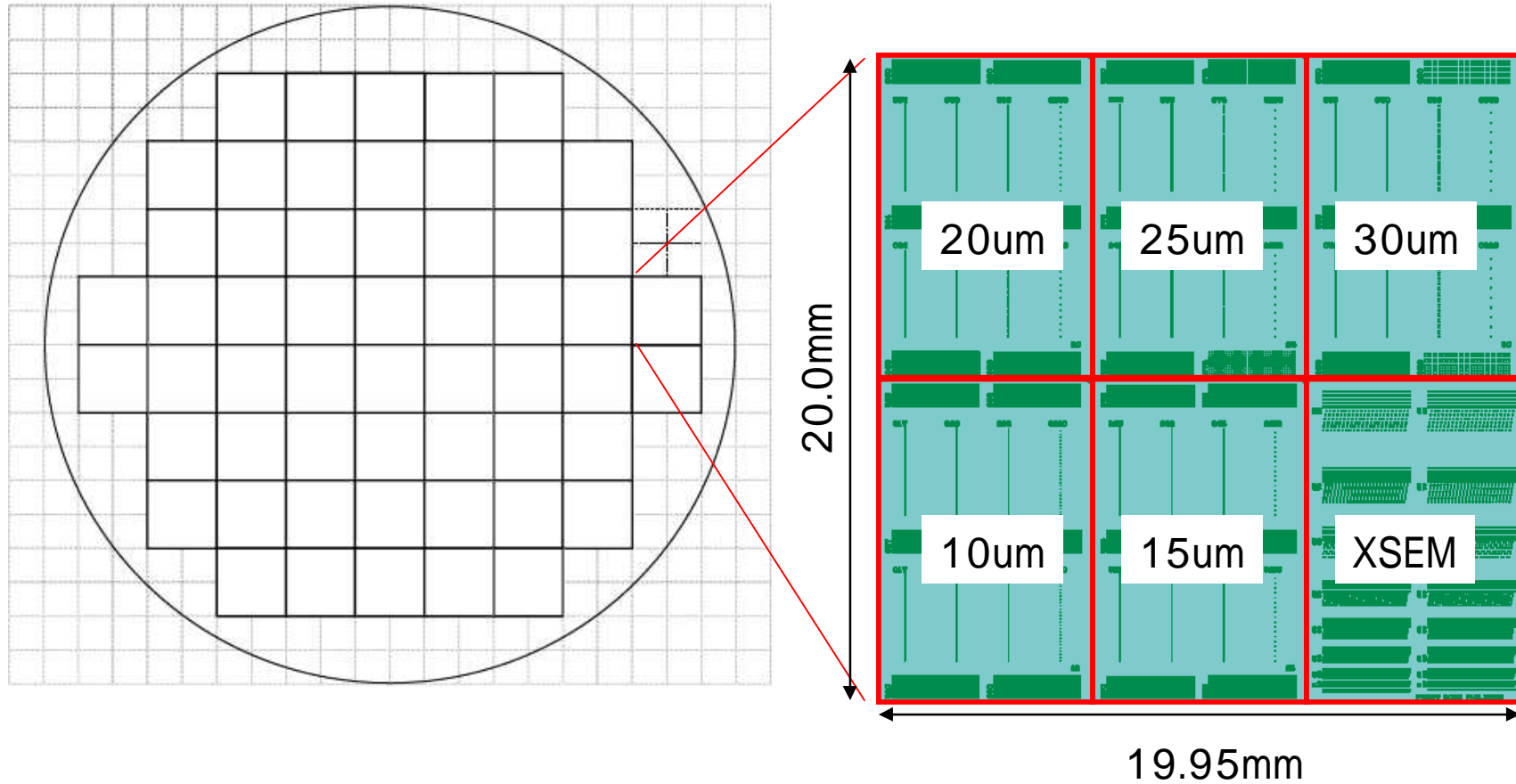
PT007 for TSV test (Cu ECP, Via First back side Polish)



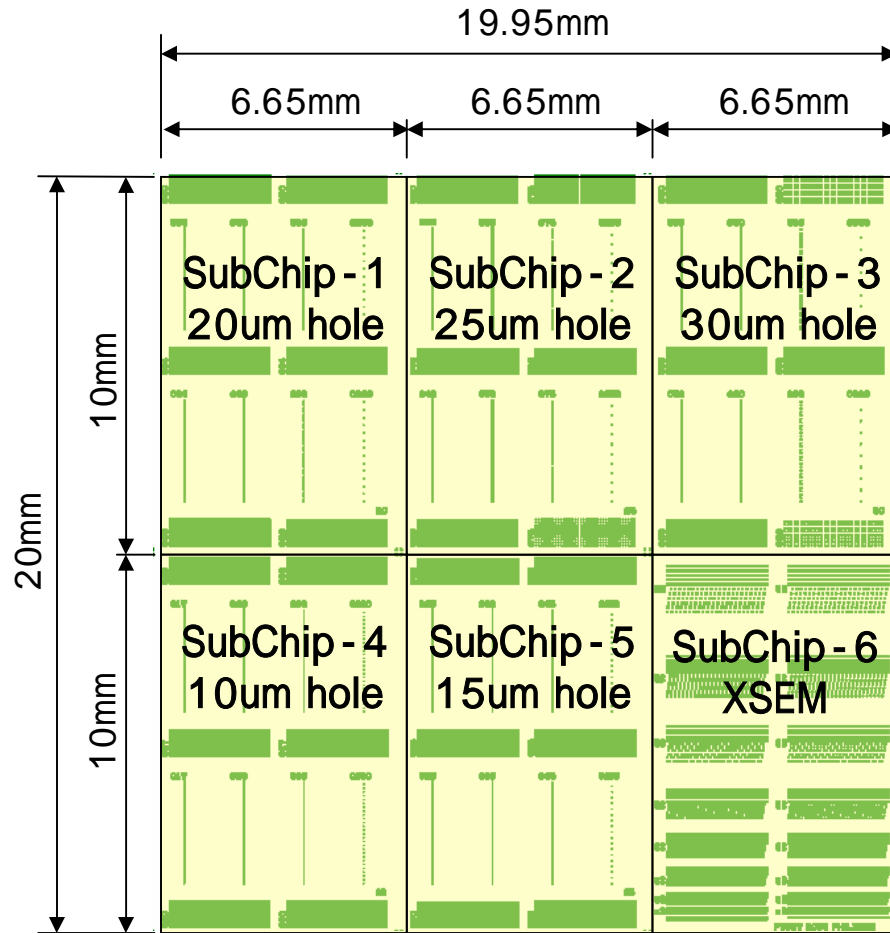
20um Hole
Cu ECP



PT007 : 200mm Shot Map

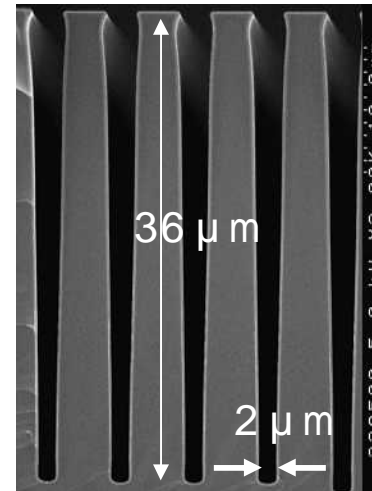


PT007 for TSV test (Cu ECP)



Chip Layout Image

- Chip Size : 19.95mm × 20mm
- Sub-Chip Size : 6.65mm × 10mm
- Feature Size :
 - 10um, 15um, 20um, 25um, 30um
 - Square & Octagon Hole pattern
- Other :
 - Density Split
 - Line & Staggered Hole for XSEM (2um ~ 40um)



2m Trench
Cu seed